CERTIFICATION OF TRANSLATION

I, ***Moung-kyo Kim***, an employee of Y.P. LEE, MOCK & PARTNERS of Koryo Building, 1575-1 Seocho-dong, Seocho-gu, Seoul, Republic of Korea 137-875, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statement in the English language in the attached translation of ***Korean Patent Application No. 10-2003-0038826*** consisting of 15 pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 16th day of May 2007

Moung kyo Kim

ABSTRACT

[Abstract of the Disclosure]

Provided are a complementary metal oxide semiconductor thin film transistor (CMOS TFT) wherein a thickness of poly silicon of a P-type TFT is greater than a thickness of poly silicon of an N-type TFT, which are formed on a substrate comprised in an active channel, and a size of a crystal grain comprised in the N-type TFT is smaller than a size of a crystal grain comprised in the P-type TFT, and a display device using the CMOS TFT. Thus, since an absolute value of a threshold voltage and current mobility can be controlled, a CMOS TFT and a flat display device that have improved electric property.

[Representative Drawing]

FIG. 1I

SPECIFICATION

[Title of the Invention]

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR THIN FILM TRANSISTOR AND DISPLAY DEVICE USING THE SAME

[Brief Description of the Drawings]

FIGS. 1a through 1i illustrate processes of fabricating a complementary metal oxide semiconductor (CMOS) TFT according to an embodiment of the present invention;

FIGS. 2a through 2c illustrate processes of fabricating a CMOS TFT according to another embodiment of the present invention; and

FIG. 3 is a graph illustrating a change in current mobility according to the size of a grain of poly silicon.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

Conventionally, circuits using a complementary metal oxide semiconductor thin film transistor (CMOS TFT) are used to drive an active matrix LCD, an organic light emitting device, an image sensor and the like. However, an absolute value of a threshold voltage of a usual TFT is greater than that of a MOS transistor using a single crystal semiconductor. In addition, an absolute value of a threshold voltage of an N-type transistor is much different from that of a P-type transistor. For example, when the absolute value of the threshold voltage of the N-type transistor is 2 V, that of the P-type transistor is -4 V.

Therefore, such difference between the absolute values of the threshold voltages of the N-type transistor and the P-type transistor is not preferable. In particular, this is

a large disadvantage for reducing a driving voltage. For example, the P-type transistor having a great threshold voltage is not appropriately driven at a low driving voltage.

That is, the P-type transistor only functions as a passive element such as a resistor, and is not operated quickly enough. To operate the P-type transistor as if a passive element, it is required for a driving voltage to be high enough.

Especially, in a case where the gate electrode is made of a material having a work function less than 5eV such as the aluminum, a difference between work functions of the gate electrode and an intrinsic silicon semiconductor is reduced as much as –0.6eV. Consequently, the threshold voltage of the P type TFT is shifted to be negative (-) value, and the threshold voltage of the N type TFT is nearly 0. That is, the N type TFT is likely rendered in an on-status.

In the above circumstances, it has been desired to approximately equalize the absolute value of a threshold voltage of the N-channel TFT to that of the P-channel TFT. In the case of conventional mono-crystalline semiconductor integrated circuit technology, the threshold voltages have been controlled by using N or P type impurity doping at a very small concentration, typically, less than 10^{18} atoms/cm^3. That is, the threshold voltages can be controlled with an accuracy of 0.1 V or less by an impurity doping at 10^{15} to 10^{18} atoms/cm^3.

However, in the case of using non-single crystalline semiconductors, even if an impurity is added at 10^{18} atoms/cm^3 or less, the shift of the threshold voltage is hardly observed. Moreover, if the concentration of the impurity exceeds 10^{18}, the threshold voltage rapidly varies and the conductivity becomes p-type or n-type. This is because polycrystalline silicon generally has a lot of defects in it. Since the defect density is 10^{18} atoms/cm^3, the added impurities are trapped by these defects and cannot be activated. Further, if the concentration of the impurity becomes larger than the defect density, the excess impurity is activated and changes the conductivity type to p-type or n-type.

In order to solve the above problems, U.S. Patent No. 6,492,268, No. 6,124,603, and No. 5,615,935 disclose a method of fabricating a channel length of the P type TFT

less than that of the N type TFT. However, according to above method, the channel lengths should vary, thus complicating the fabrication processes.

[Technical Goal of the Invention]

The present invention relates to a complementary metal oxide semiconductor thin film transistor (CMOS TFT) and a display device using the same, and more particularly, to a CMOS TFT in which absolute values of threshold voltages of a P-type transistor and an N-type transistor are almost similar and current mobility is high, and a display device using the CMOS TFT.

[Structure and Operation of the Invention]

According to an aspect of the present invention, it is provided is a complementary metal oxide semiconductor thin film transistor (CMOS TFT) wherein a thickness of poly silicon of a P-type TFT is greater than a thickness of poly silicon of an N-type TFT, which are formed on a substrate comprised in an active channel, and a size of a crystal grain comprised in the N-type TFT is smaller than a size of a crystal grain comprised in the P-type TFT.

According to an aspect of the present invention, it is provided is a CMOS TFT including: a substrate; a buffer layer; and a P-type TFT and an N-type TFT comprising a poly silicon layer formed on the buffer layer, wherein the P-type TFT further comprises an insulating layer formed between the substrate and the buffer layer.

According to an aspect of the present invention, it is provided is a display device in which the CMOS TFT is used, which is a liquid crystal display device or a organic light emitting display device.

Preferred embodiments of the present invention will now be described with reference to the attached drawings.

Since the crystal grain size of the polycrystalline silicon included in the active area affects the electronic properties of the TFT, that is, the current mobility and the threshold voltage, the electronic properties of the CMOS TFT can be improved by

controlling the crystal grain sizes of the polycrystalline silicon included in the P type TFT and N type TFT of the CMOS TFT.

FIGS. 1a through 1i are views of processes for fabricating the CMOS TFT.

As shown in FIG. 1a, a buffer layer 11 is deposited on a substrate 10 including N type TFT region 10a and P type TFT region 10b. SiO_2 can be used as the buffer layer 11. After depositing the buffer layer 11, the amorphous silicon 12 is deposited on the buffer layer 11. Here, the amorphous silicon is deposited to have a thickness of 500 to 1500 Å.

As shown in FIG. 1b, a photoresist pattern 13 is formed on the amorphous silicon 12 on the N type TFT region 10a, and the amorphous silicon is dry-etched. Then, the amorphous silicon 12b on the P type TFT region 10b is etched as deep as a predetermined depth, the thickness of the amorphous silicon 12a and the amorphous silicon 12b become different from each other.

Here, the thickness of the amorphous silicon 12b remained on the P type TFT is about 300 to 800Å.

After removing the photoresist 13, the laser is radiated to the amorphous silicon to crystallize the amorphous silicon into the polycrystalline silicon as shown in FIG. 1c. Here, since the thickness of the amorphous silicon 12b on the P type TFT region 10b is thinner than that of the amorphous silicon 12a on the N type TFT region 10b, the amorphous silicon 12b on the P type TFT region 10b is crystallized after being melted completely, and the amorphous silicon 12a on the N type TFT region 10a is crystallized after being melted partially. Therefore, the crystal grain size of the polycrystalline silicon formed on the P type TFT region 10b becomes larger, and the crystal grain size of the polycrystalline silicon formed on the N type TFT region 10a is smaller than that of the P type TFT region 10b.

Here, since the crystal grain size of the P type TFT region 10b is larger than that of the N type TFT region 10a, less grain boundaries are included in the P type TFT region 10b.

On the other hand, when the amorphous silicon is crystallized using the laser,

grain boundaries are formed between the grains. The grain boundaries affect the current mobilities and the threshold voltages of the P type TFT and the N type TFT, when the device is fabricated. That is, the grain boundary is operated as a trap with respect to electric charge carriers.

FIG. 3 is a graph illustrating a change in current mobility according to the size of a grain of poly silicon. As shown in FIG. 3, as the grain size becomes larger, the current mobility increases.

Therefore, since the number of grain boundaries included in the P type TFT region is small, the current mobility increases and the threshold voltage is reduced relatively on the N type TFT region. Thus, the difference between the electronic properties of the P type TFT and the N type TFT is reduced.

Here, widths of the channel regions of the N type TFT and the P type TFT are formed to be same as each other.

O the other hand, it is desirable that the laser eximer annealing (ELA) method is used as the laser crystallization method, and the laser of 320mJ/cm^2 energy is used.

As shown in FIG. 1d, after forming the polycrystalline silicon pattern, the polycrystalline silicon pattern 12a of the N type TFT region 10a is exposed to make the N type TFT conductive, and the channel doping is performed to be N type dopant using the patterned photoresist 14 as a mask.

The N type TFT can be formed to have a general N type TFT structure, a lightly doped drain (LDD) structore, or an off-set structure, and is not limited to a certain structure. In the present invention, the processes will be described with respect to the CMOS TFT having the LDD structure.

As shown in FIG. 1e, the photoresist 14 is removed, a gate insulating layer 15 is formed on the substrate 10, and gate electrode material is deposited on the gate insulating layer 15. In addition, gate electrodes 16a and 16b of the N type TFT and P type TFT are formed on the substrate 10 using the mask. In order to form the LDD structure, impurities of low concentration is ion-implanted into the polycrystalline silicon pattern 12a of the N type TFT region 10a to form source/drain area 17 of low

concentration on both sides of the gate electrode 16a.

As shown in FIG. 1f, the photoresist is applied on the entire surface of the substrate 10, on which the low concentration source/drain area 17 is formed, after that, the photolithography process is performed to prevent the impurities from being injected into the N type TFT region 10a and to form the mask for forming source/drain area of the P type TFT. The P type impurities of high concentration is ion-implanted into the polycrystalline silicon pattern 12b of the P type TFT region 10b using the mask to form high concentrated source/drain area 19.

As shown in FIG. 15g, the photoresist pattern is applied on the substrate 10 after removing the mask, and the photolithograph process is performed to form the gate electrode and the mask 20, which prevents the impurities from being injected into the P type TFT region 10a. In addition, N type high concentrated impurities are ion-implanted into the polycrystalline pattern 12a of the N type TFT region 10a using the mask 20 to form high concentrated source/drain area 19.

As shown in FIG. 1h, an interlayer dielectrics 22 is formed on the entire surface of the substrate 10 after removing the mask 20. Then, the mask is located on the substrate 10 to etch the interlayer dielectrics 22 so as to expose the source/drain areas 19 and 21 of the N type TFT and P type TFT and to form contact holes 23a and 23b on the N type TFT region 10a and the P type TFT region 10b.

In addition, as shown in FIG. 1i, conductive metallic material is deposited on the entire surface of the substrate 10 to form source/drain electrodes, and the metallic material is etched using the mask to form the source/drain electrodes 24a and 24b of the N type TFT and the P type TFT.

The CMOS TFT having the N type TFT of LDD structure and the P type TFT of general structure can be fabricated as described above.

On the other hand, FIGS. 2a through 2c illustrate different crystal grain sizes of the polycrystalline silicon formed on the polycrystalline silicon patterns 12a and 12b of the P type TFT region and the N type TFT region.

Referring to FIGS. 2a through 2c, an insulating layer 25 such as SiNx is formed

on the P type TFT region 10b, on which the P type TFT is formed. As shown in FIG. 2b, the buffer layer 11 is formed on the entire surface of the substrate 10. SiO_2 can be used as the buffer layer 11. The amorphous silicon is deposited uniformly on the entire substrate 10, and after that, the amorphous silicon is crystallized by the laser using the mask to form the polycrystalline silicon patterns 12a and 72b.

Here, since the insulating layer such as SiNx is applied on the lower portion of the P type TFT, the energy of the radiated laser is less transmitted than that of the N type TFT region. That is, since the heat conductivity of the P type TFT is smaller than that of the N type TFT, the energy affecting the amorphous silicon on the P type TFT region is larger than that of the N type TFT region, and the P type transistor region is melted more than the N type TFT region. Therefore, the crystal grain size of the P type TFT region is larger than that on the N type TFT region. Thus the difference between electronic properties of the P type TFT and the N type TFT is reduced.

The ELA method is used as the laser crystallization method, and the laser of $320mJ/cm^2$ is used.

Processes after the above process are same as those shown in FIGS. 1d through 1i.

As described above, the CMOS TFT, in which the crystal grain size of the polycrystalline silicon on the active channel region of the N type TFT is smaller than that of the P type TFT is used in the display devices, and more preferably, used in the active device type LCD or the organic electroluminescence device.

[Effect of the Invention]

The absolute values of the threshold voltages and the current mobility can be controlled by differentiating the crystal grain sizes on the N type TFT and the P type TFT included in the CMOS TFT, thus improving electronic properties of the CMOS TFT.

What is claimed is:

1. A CMOS TFT (complementary metal oxide semiconductor thin film transistor) wherein a thickness of poly silicon of a P-type TFT is greater than a thickness of poly silicon of an N-type TFT, which are formed on a substrate comprised in an active channel, and a size of a crystal grain comprised in the N-type TFT is smaller than a size of a crystal grain comprised in the P-type TFT.

2. The CMOS TFT of claim 1, wherein the thickness of the poly silicon of the P-type TFT is in the range of 300 to 800 Å.

3. The CMOS TFT of claim 1, wherein the thickness of the poly silicon of the N-type TFT is in the range of 500 to 1500 Å.

4. The CMOS TFT of claim 1, wherein the poly silicon is manufactured using eximer laser annealing crystallization.

5. The CMOS TFT of claim 1, wherein the CMOS TFT comprises a LDD structure or off-set structure.

6. A CMOS TFT comprising:

a substrate;

a buffer layer; and

a P-type TFT and an N-type TFT comprising a poly silicon layer formed on the buffer layer,

wherein the P-type TFT further comprises an insulating layer formed between the substrate and the buffer layer.

7. The CMOS TFT of claim 6, wherein the buffer layer is formed of SiO_2 and the insulating layer is formed of SiN_x.

8. The CMOS TFT of claim 6, wherein the poly silicon is manufactured using eximer laser annealing crystallization.

9. The CMOS TFT of claim 6, wherein the CMOS TFT comprises a LDD structure or off-set structure.

10. A display device in which the CMOS TFT of claim 1 or 6 is used.

11. The display device of claim 10, wherein the display device is a liquid crystal display device or an organic light emitting display device.

FIG. 1A

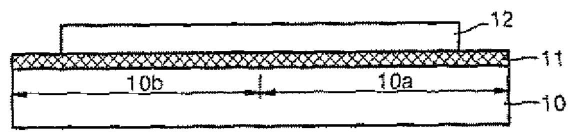


FIG. 1B

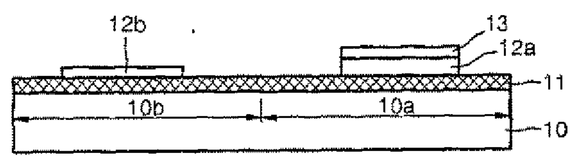


FIG. 1C

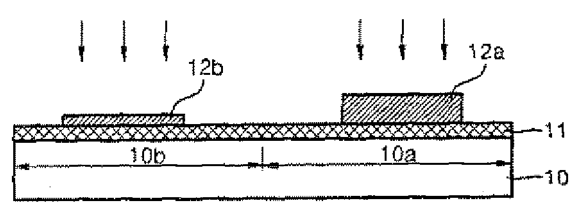


FIG. 1D

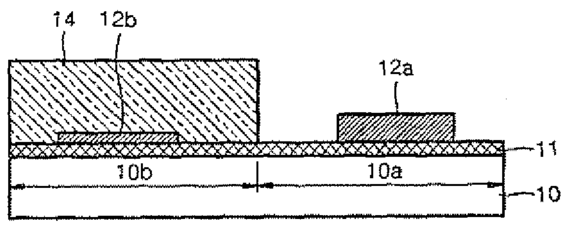


FIG. 1E

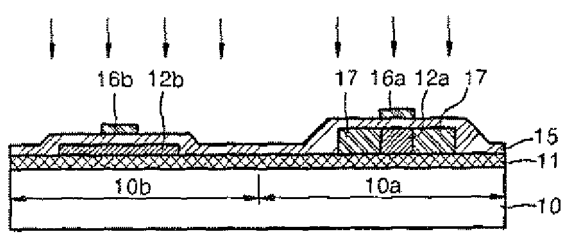


FIG. 1F

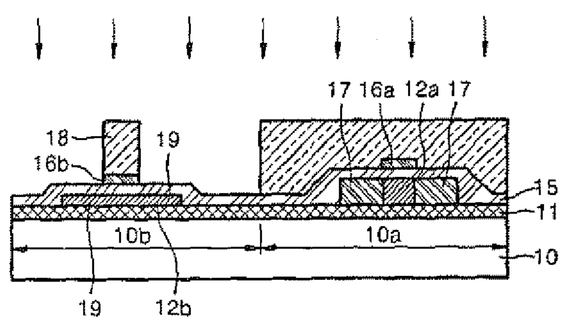


FIG. 1G

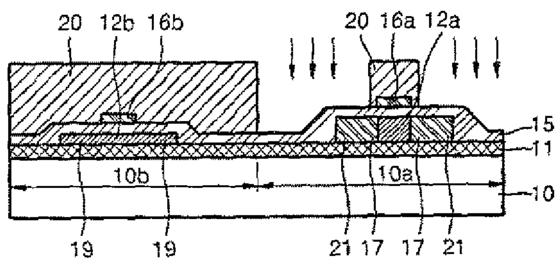


FIG. 1H

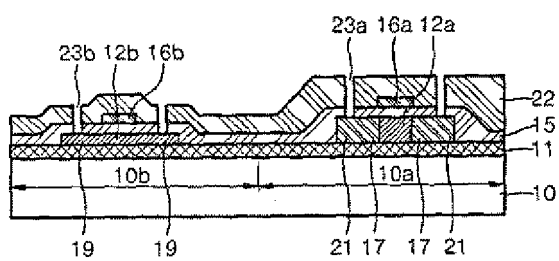


FIG. 1I

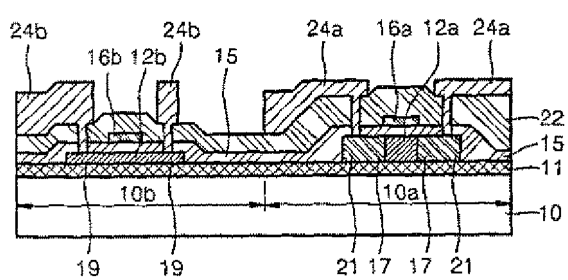


FIG. 2A

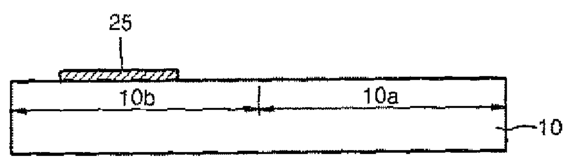


FIG. 2B

FIG. 2C

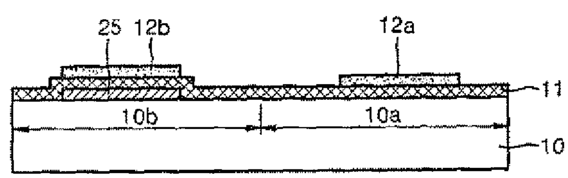
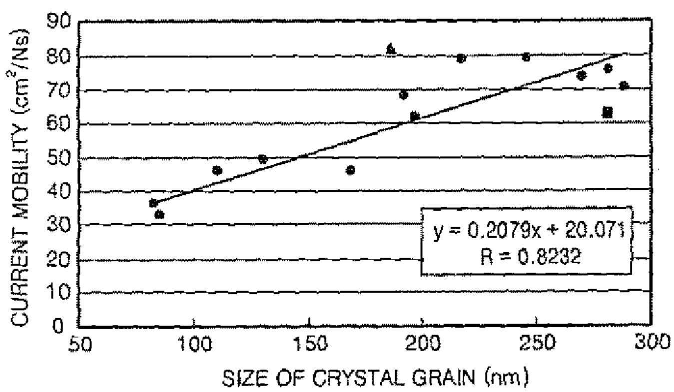


FIG. 3



CURRENT MOBILITY (cm^2/Ns)
90
80
70
60
50
40
30
20
10
0
50
100
150
200
250
300
SIZE OF CRYSTAL GRAIN (nm)
y = 0.2079x + 20.071
R = 0.8232